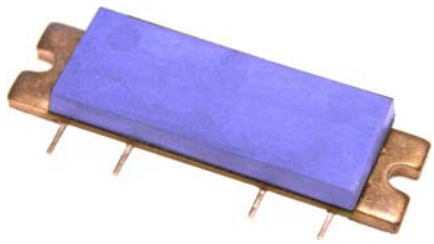
XD010-12S-D4F
XD010-12S-D4FY

RoHS Compliant & Green Package

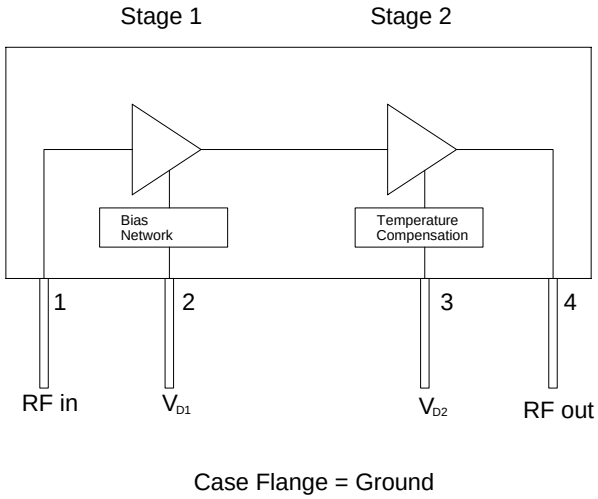
869-894 MHz Class AB
15W Power Amplifier Module



Product Description

Sirenza Microdevices' **XD010-12S-D4FY** is a 15 Watt, 2-Stage class A/AB LDMOS power amplifier module designed for use in the 869-894 MHz frequency band. The module is internally matched to 50 ohms and operates directly from 28V making system integration very simple. Internal gate bias temperature compensation circuitry ensures consistent unit-to-unit performance over the full operating temperature range. The XD010-12S-D4FY offers a rugged class 3B HBM ESD rating (>8000V).

Functional Block Diagram



Case Flange = Ground

Product Features

- **50 Ω RF impedance, Fully Integrated Matching**
- **15W Output P_{1dB}**
- **Single Supply Operation : Nominally 28V**
- **High Gain: 32 dB at 880 MHz**
- **Internal Gate Bias Temperature Compensation**
- **Power up/down control < 1μs**
- **ESD Rating (HBM): Class 3B (8000 V)**

Applications

- **Base Station PA driver**
- **Repeater**
- **CDMA / WCDMA**
- **GSM / EDGE**

Key Specifications

Symbol	Parameter	Unit	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	869	-	894
P_{1dB}	Output Power at 1dB Compression, 880MHz	W	12	15	-
Gain	Gain at 1W Output Power, 880MHz	dB	30	32	-
Gain Flatness	Peak to Peak Gain Variation, 869 - 894MHz	dB	-	0.2	1.0
IRL	Input Return Loss 1W Output Power, 869 - 894MHz	dB	14	17	-
Efficiency	Drain Efficiency at 12W CW, 880MHz	%	27	33	-
	Drain Efficiency at 2W CDMA (Single Carrier IS-95)	%	-	12	-
	Drain Efficiency at 1W CDMA (Single Carrier IS-95)	%	-	7	-
Linearity	ACPR at 2W CDMA (Single Carrier IS-95, 9 Ch Fwd, Off-set=750KHz, ACPR Integrated Bandwidth), 880MHz	dB	-	-51	-
	ALT-1 at 2W CDMA (Single Carrier IS-95, 9 Ch Fwd, Offset=1980KHz, ACPR Integrated Bandwidth), 880MHz	dB	-	-70	-
	3^{rd} Order IMD at 12W PEP (Two Tone), 880MHz	dBc	-	-34	-30
	3^{rd} Order IMD at 1W PEP (Two Tone), 880MHz	dBc	-	-45	-
Delay	Signal Delay from Pin 1 to Pin 4	nS	-	2.5	-
Phase Linearity	Deviation from Linear Phase (Peak to Peak)	Deg	-	0.5	-
$R_{TH, j-l}$	Thermal Resistance Stage 1 (Junction to Case)	ºC/W	-	11	-
$R_{TH, j-2}$	Thermal Resistance Stage 2 (Junction to Case)	ºC/W	-	4	-

Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_D = 28.0V$, $I_{DQ1} = 230$ mA, $I_{DQ2} = 150$mA, $T_{Flange} = 25ºC$

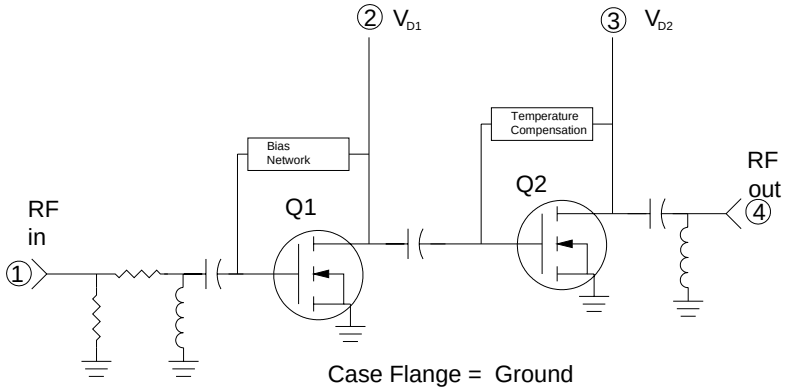
Quality Specifications

Parameter		Unit	Typical
ESD Rating	Human Body Model, JEDEC Document - JESD22-A114-B	V	8000
MTTF	85°C Leadframe, 200°C Channel	Hours	1.2 X 10^6

Pin Description

Pin #	Function	Description
1	RF Input	Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
2	V_{D1}	This is the drain voltage for the first stage. Nominally +28Vdc
3	V_{D2}	This is the drain voltage for the 2nd stage of the amplifier module. The 2nd stage gate bias is temperature compensated to maintain constant quiscent drain current over the operating temperature range. See Note 1.
4	RF Output	Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
Flange	Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions in application note AN-060 on Sirenza's web site.

Simplified Device Schematic



Absolute Maximum Ratings

Parameters	Value	Unit
1st Stage Bias Voltage (V_{D1})	35	V
2nd Stage Bias Voltage (V_{D2})	35	V
RF Input Power	+20	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Output Device Channel Temperature	+200	ºC
Operating Temperature Range	-20 to +90	ºC
Storage Temperature Range	-40 to +100	ºC

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Note 1:
The internally generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be accomplished with AGC external to the module.

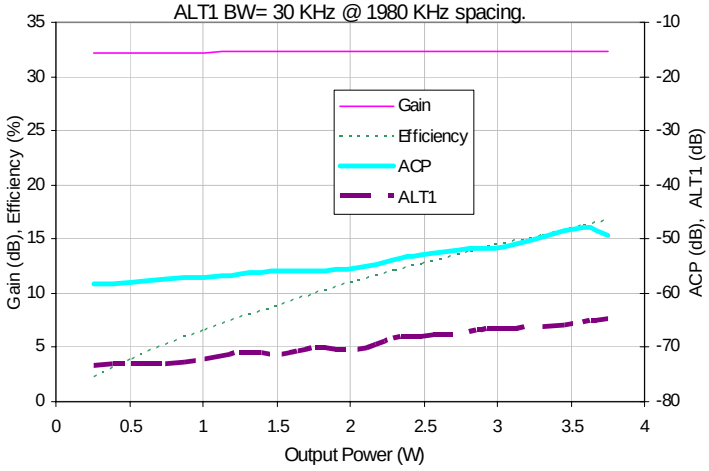
Note 2:
Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

Note 3:
This module was designed to have its leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° F, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN060 (www.sirenza.com) for further installation
instructions.

Typical Performance Curves

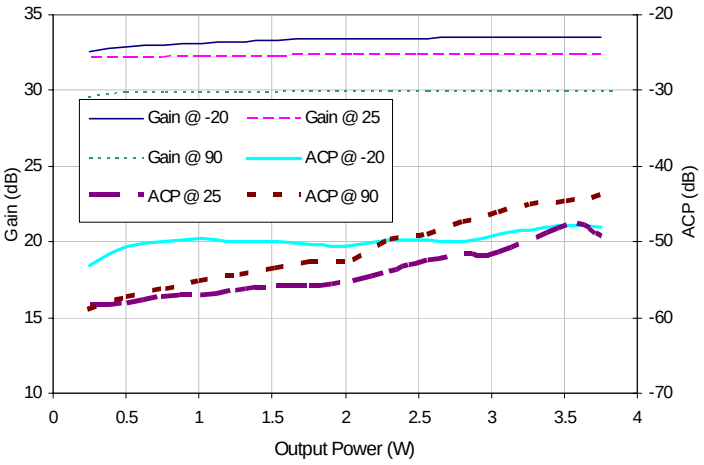
Gain, Efficiency, ACP, ALT1 vs. Output Power

Freq=881 MHz, Vdd=28 V, T_{Flange}=25 °C
IS95 standard, channel BW= 1.23 MHz.
ADJ BW= 30 KHz @ 750 KHz spacing.
ALT1 BW= 30 KHz @ 1980 KHz spacing.



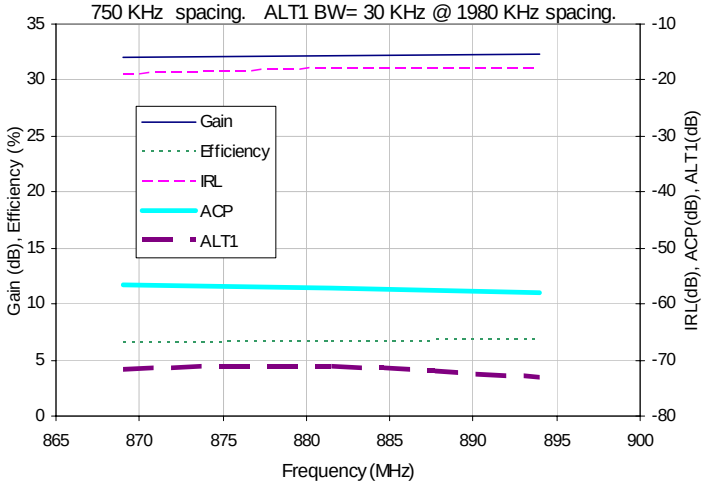
Gain, ACP vs. Output Power over Temperature

Freq=881 MHz, Vdd=28 V, T_{Flange}=-20 °C, 25 °C, 90 °C
IS95 standard, channel BW= 1.23 MHz. ADJ BW= 30 KHz @ 750 KHz spacing. ALT1 BW= 30 KHz @ 1980 KHz spacing.



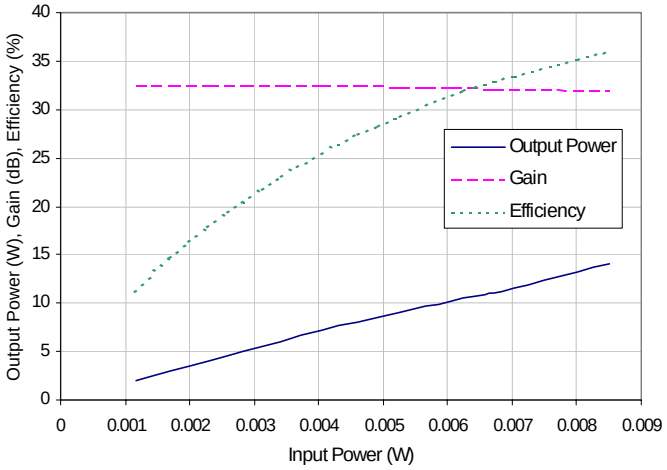
Gain, Efficiency, IRL, ACP, ALT1 vs. Frequency

Output Power= 1 Watt Vdd=28 V, T_{Flange}=25 °C
IS95 standard, channel BW= 1.23 MHz. ADJ BW= 30 KHz @ 750 KHz spacing. ALT1 BW= 30 KHz @ 1980 KHz spacing.



Output Power, Gain, Efficiency vs. Input Power

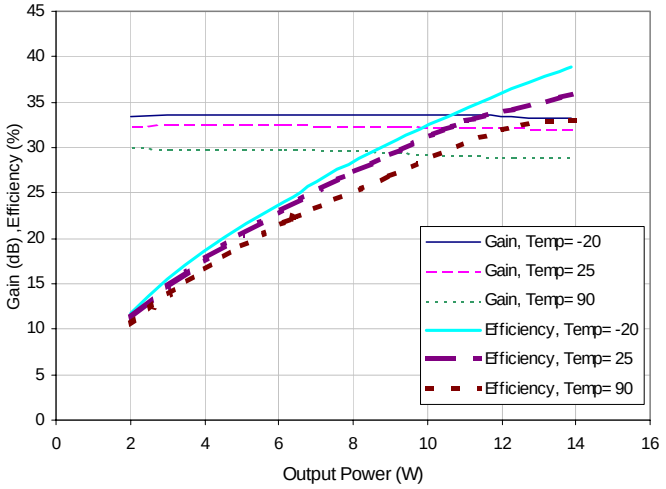
Freq=881 MHz, Vdd=28 V, T_{Flange}=25°C



Typical Performance Curves (cont'd)

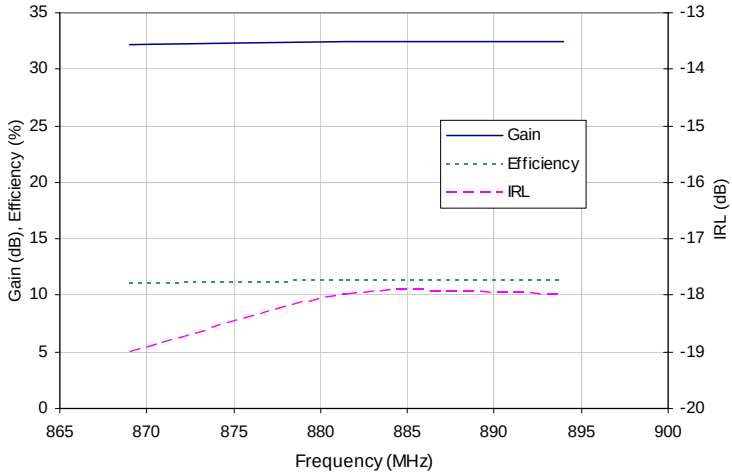
Gain, Efficiency vs. Output Power over Temperature

Freq=881 MHz, Vdd=28 V, T_{Flange}=-20 °C, 25 °C, 90 °C

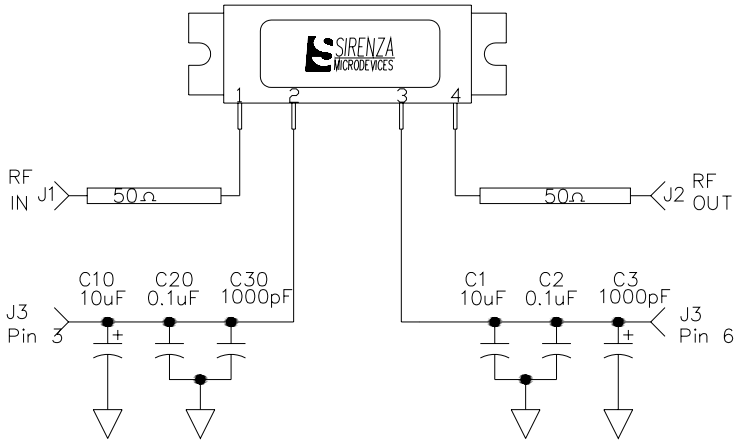


Gain, Efficiency, IRL vs. Frequency

Output Power=1 Watt, Vdd=28 V, T_{Flange}=25 °C



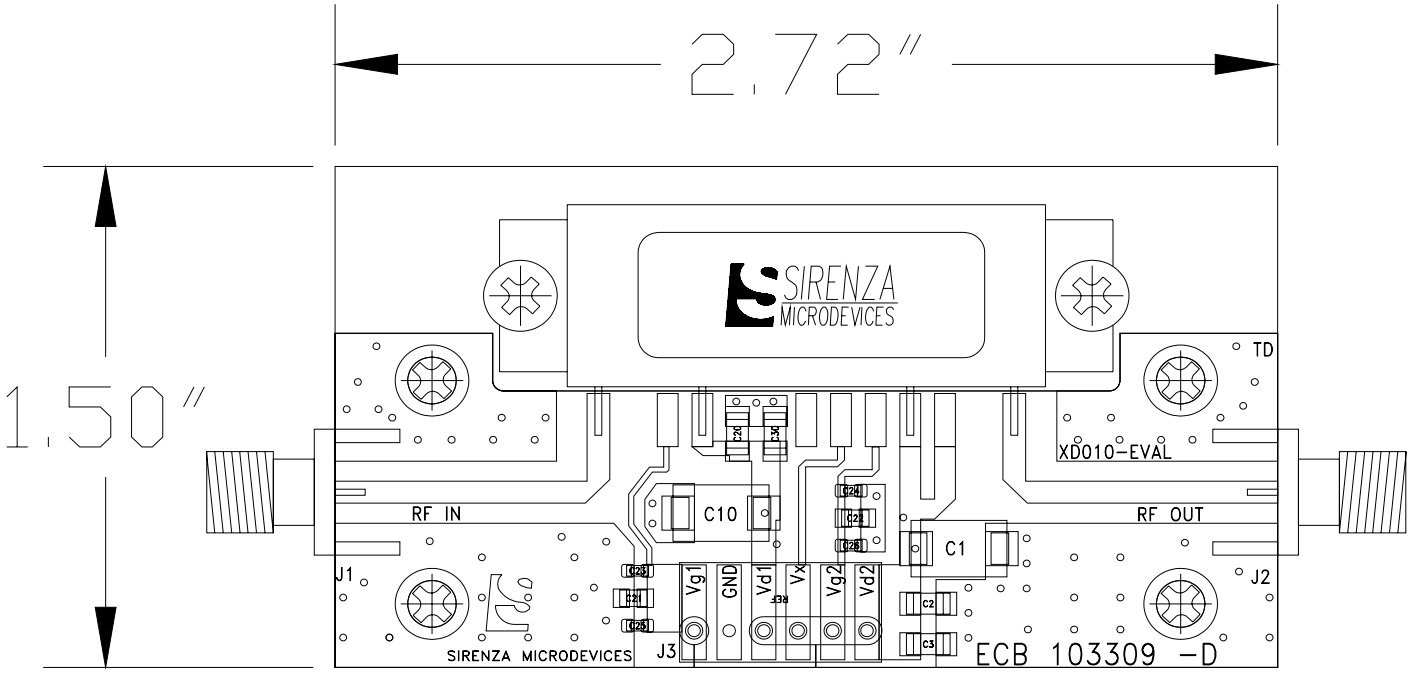
Test Board Schematic with module connections shown



Test Board Bill of Materials

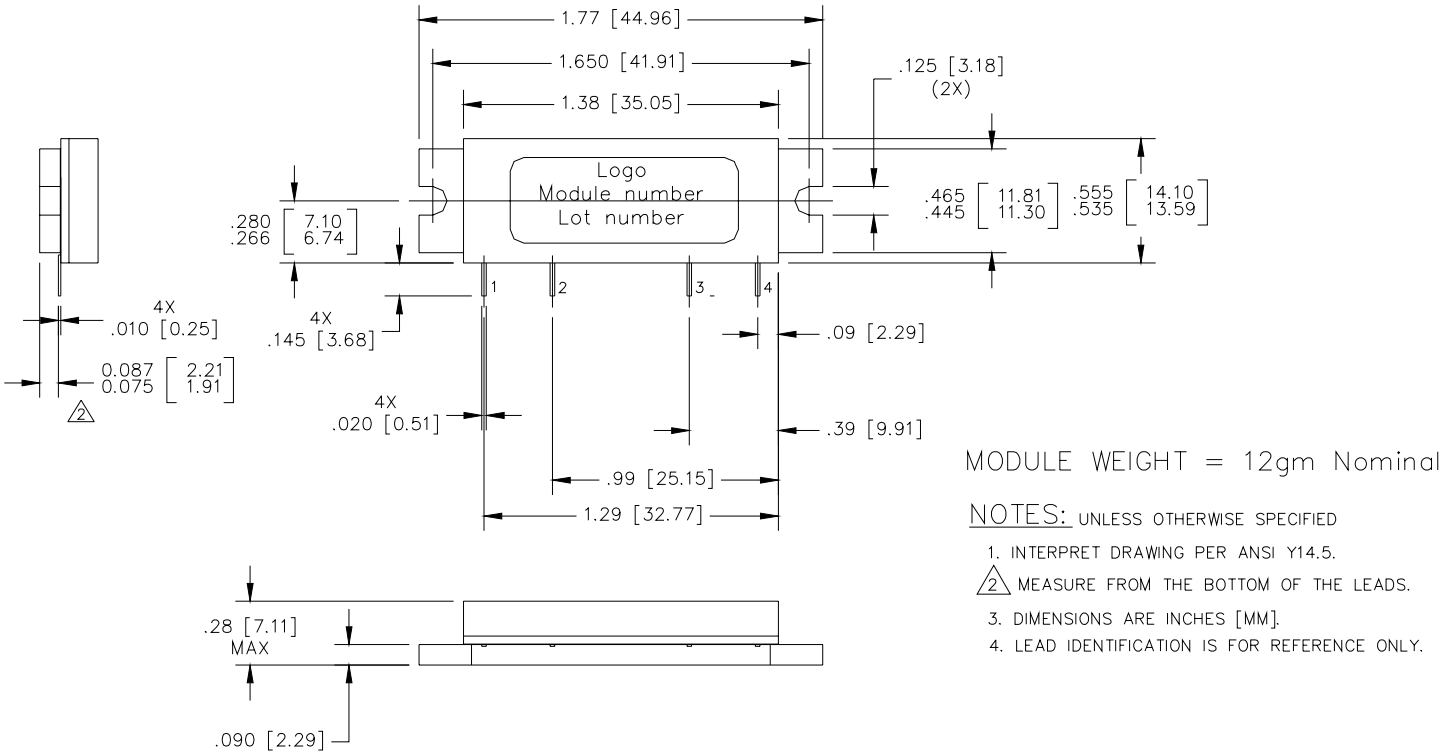
Component	Description	Manufacturer
PCB	Rogers 4350, ε_r=3.5 Thickness=30mils	Rogers
J1, J2	SMA, RF, Panel Mount Tab W / Flange	Johnson
J3	MTA Post Header, 6 Pin, Rect-angle, Polarized, Surface Mount	AMP
C1, C10	Cap, 10μF, 35V, 10%, Tant, Elect, D	Kemet
C2, C20	Cap, 0.1μF, 100V, 10%, 1206	Johanson
C3, C30	Cap, 1000pF, 100V, 10%, 1206	Johanson
C25, C26	Cap, 68pF, 250V, 5%, 0603	ATC
C21, C22	Cap, 0.1μF, 100V, 10%, 0805	Panasonic
C23, C24	Cap, 1000pF, 100V, 10%, 0603	AVX
Mounting Screws	4-40 X 0.250”	Various

Test Board Layout

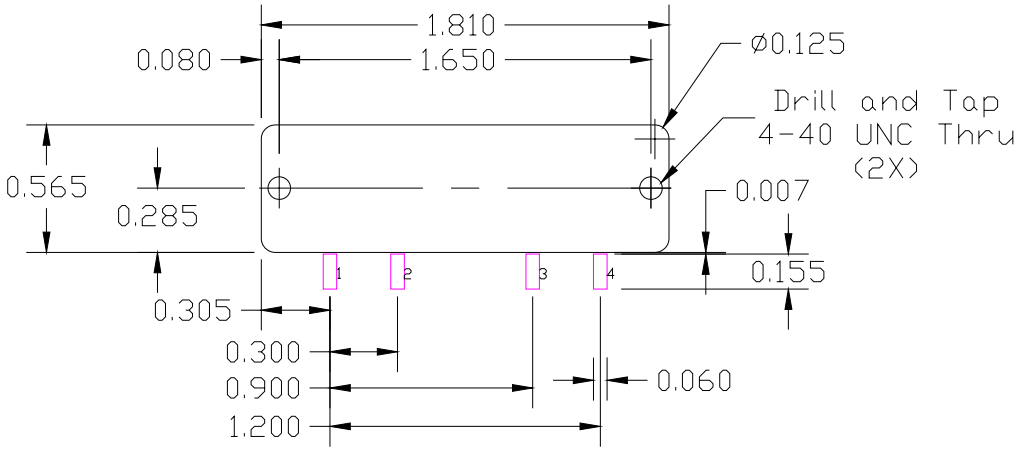


To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com. Data sheet for evaluation circuit (XD010-EVAL) available from Sirenza website.

Package Outline Drawing



Recommended PCB Cutout and Landing Pads for the D4F Package



Note 3: Dimensions are in inches

Refer to Application note AN-060 “Installation Instructions for XD Module Series” for additional mounting info. App note availbale at at www.sirenza.com